IDEC Chip Design Contest

Mixed-Signal Neural Network Inference Processor in 28-nm

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INTRODUCTION

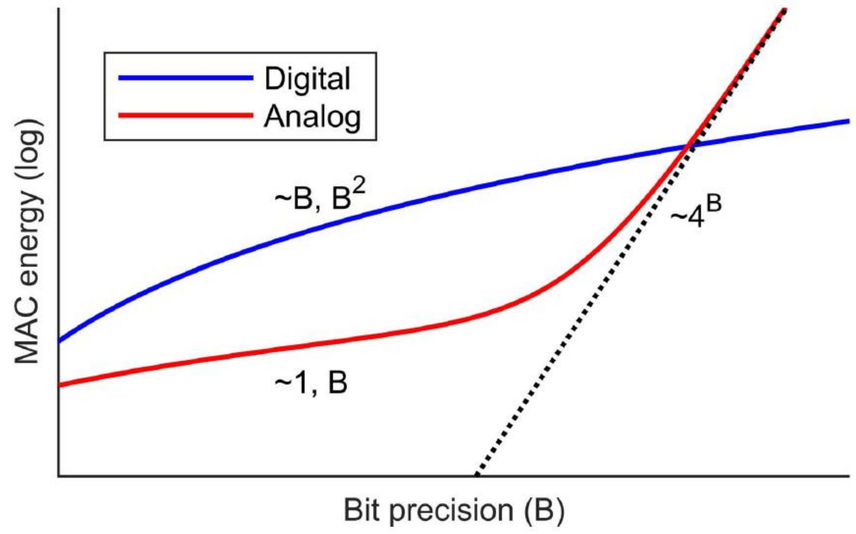

Fig. 1. Comparison of power consumption between analog and digital circuits according to SNR requirements [1].

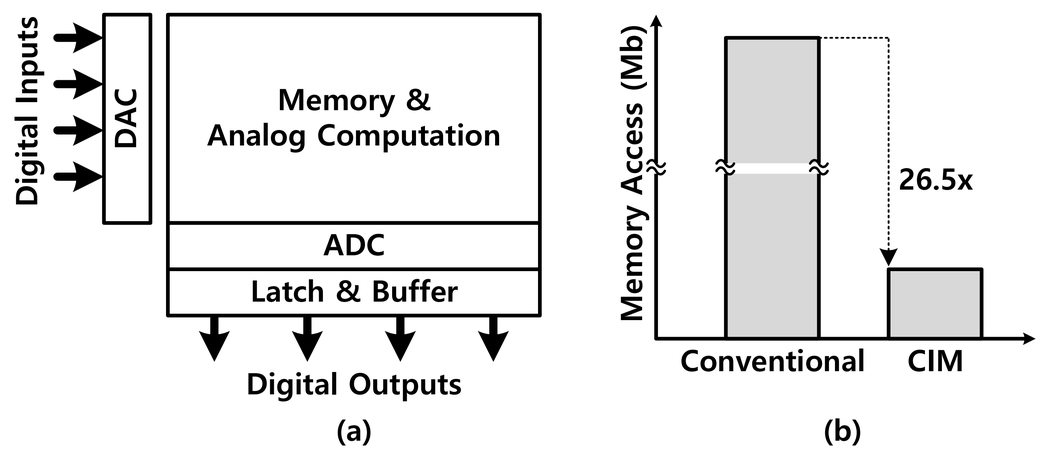

Fig. 2. (a) Conventional CIM Architecture; (b) Memory access reduction [2]

[1] B. Murmann, IEEE Transactions on VLSI Systems, Vol. 29, Jan. 2021
[2] Zheyu Liu et al., IEEE Transactions on Circuits and Systems I, Vol. 67, Sep. 2020

SYSTEM ARCHITECTURE AND EXPERIMENTAL RESULTS

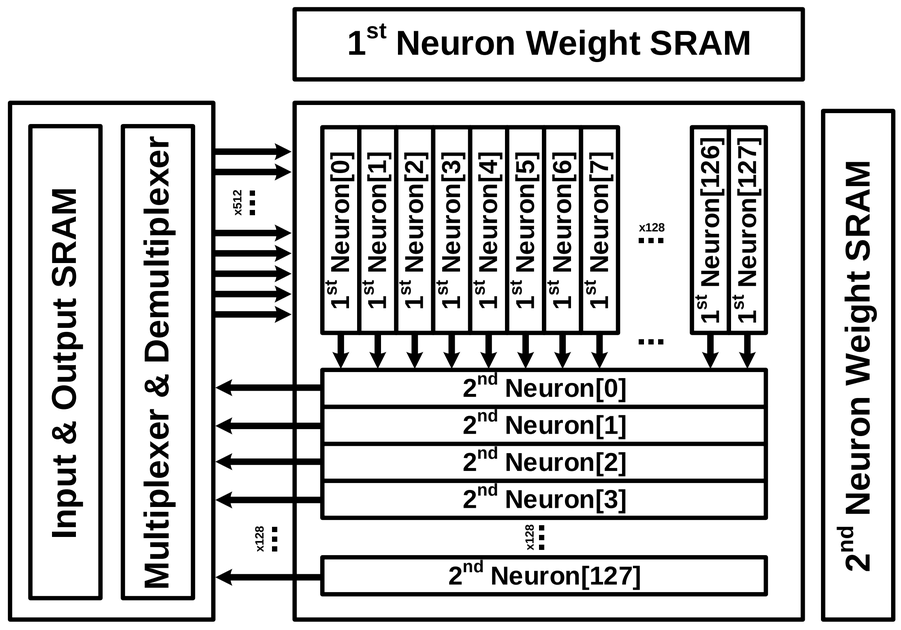

Fig. 3. Overall architecture

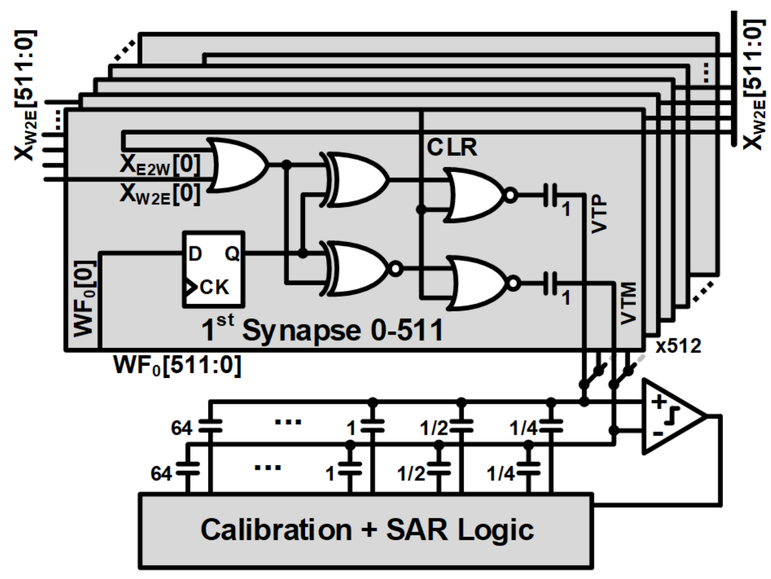

Fig. 4. SAR ADC with calibration logic for the proposed neural network architecture.

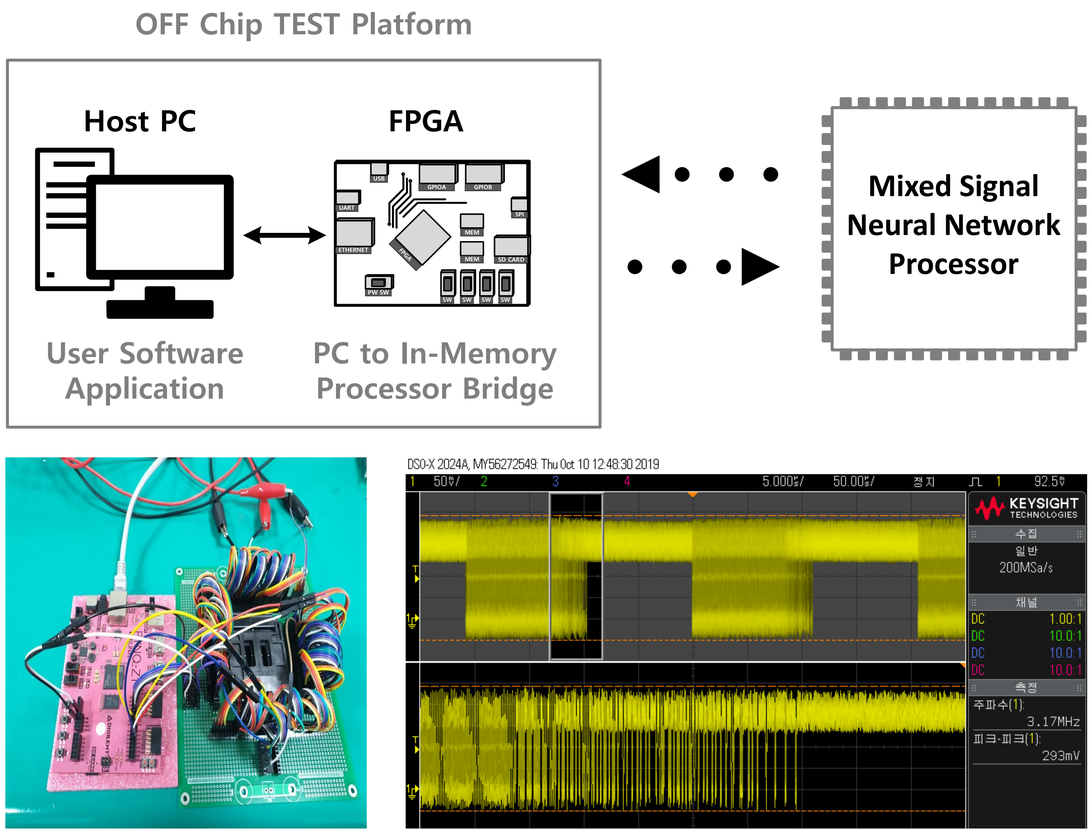

Fig. 5. Demo system and measured waveform

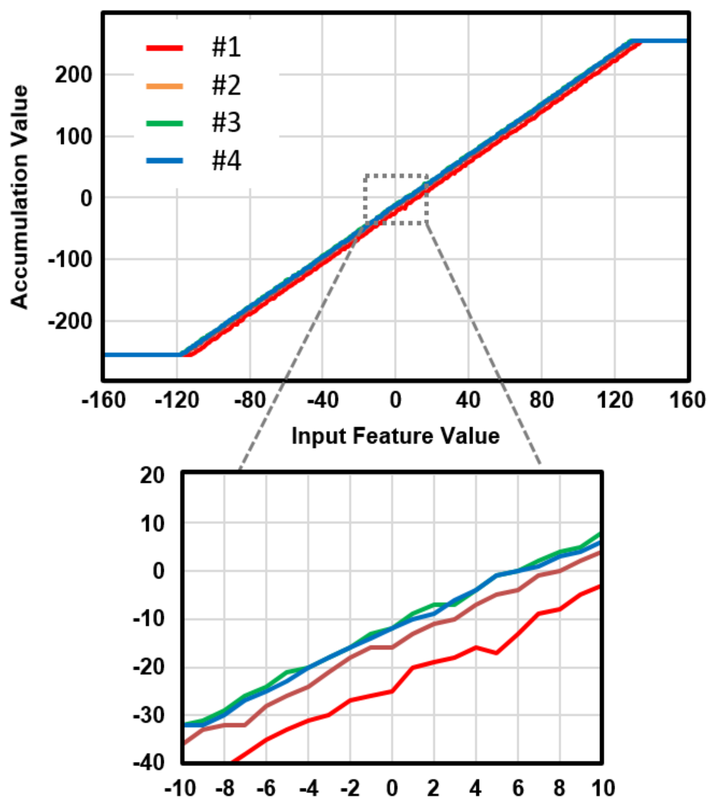

Fig. 6. Measured transfer function

Acknowledgement: The chip fabrication was supported by the IC Design Education Center(IDEC), Korea.

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